1W,28V Plastic RF LDMOS Gain Block

ITEH40001P3

Description

The ITEH40001P3 is a 1-watt, highly rugged, high linear, LDMOS gain block, designed for any applications at frequencies up to 4GHz, in 6*5mm DFN plastic package, supporting surface mounted on PCB through high density grounding vias.

General broadband reference design:

- Sub 1GHz VHF and UHF: 100-1000MHz
- L band 1-2GHz
- S band: 2-3GHz, 3-4GHz

*：Narrower band reference design upon request

Suitable Applications

- Driver or pre-driver of PA lineup
- 2nd or 3rd stage of LNA lineup

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, Pout=1W 2.1GHz	RθJC	20	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

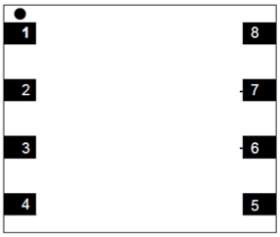
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA

Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 28V, I_D = 70mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.8	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 70 mA, f = 2100 MHz

VSWR 10:1 at 1W pulse CW Output Power	No Device Degradation

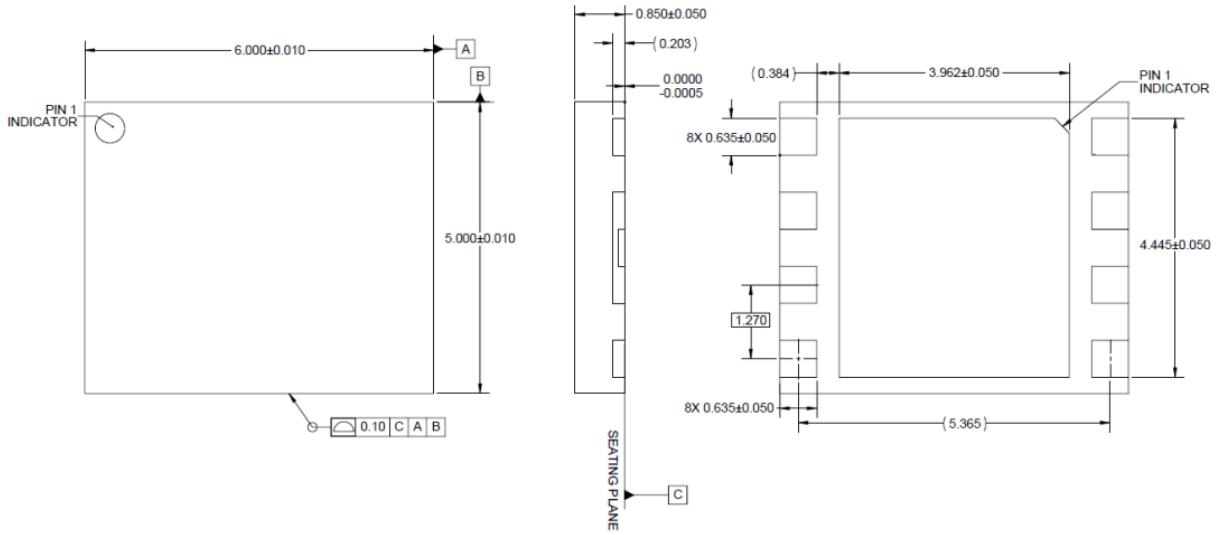
Pin Configuration and Description(Top view)



Pin No.	Symbol	Description
1,2,3,4	RF IN/VGS	Gate Bias/RF Input
5,6, 7,8	RF OUT /VDS	RF Output, Drain Bias
Backside metal	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

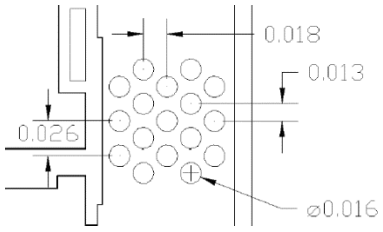
Package

6*5 DFN Package



Notes:
1. All dimensions are in mm. Otherwise noted, the tolerance is ±0.1 mm.
2. Package leads are gold plated.
3. Part is mold encapsulated.

Recommended vias layout: (all in inches)



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2024/9/11	Rev 1.0	Preliminary Datasheet

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