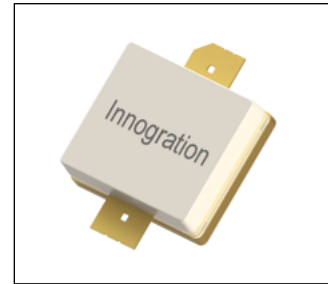


150W, 50V High Power RF LDMOS FETs

Description

The ITEV01150A2C is a 150-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 500MHz, in new generation highly cost effective open cavity package. It is featured by single ended configuration for high power and high ruggedness, suitable for Industrial, Scientific and Medical application



- Typical performance(on Innogrations test board with device soldered)

Signal: CW , $V_{gs}=3.4V, V_{ds}=50V, I_{dq}=100mA$

Freq (MHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Ids (A)	Gain (dB)	Eff (%)	2 nd harmonic (dBc)
40.68	32	52	160	4.1	20	78	-20

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+135	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c=85^\circ C, T_j=200^\circ C, DC$ test	$R_{\theta JC}$	0.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

ITEV01150A2C LDMOS TRANSISTOR

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Table 4. Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage $V_{GS}=0, I_{DS}=1.0\text{mA}$	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$)	I_{loss}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$)	I_{loss}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{V}, V_{DS} = 0\text{V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{V}, I_D = 600\text{ }\mu\text{A}$)	$V_{GS(th)}$	—	2.65	—	V
Gate Quiescent Voltage ($V_{DD} = 50\text{V}, I_D = 180\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.4	—	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 50\text{Vdc}$, $I_{DQ} = 100\text{mA}$, $f = 100\text{MHz}$, pulse width:100us, duty cycle:10%

Load 65:1 All phase angles, at 150W Pulsed CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

Figure 1: CW Gain and Power Efficiency as a Function of Pout at 40.68MHz

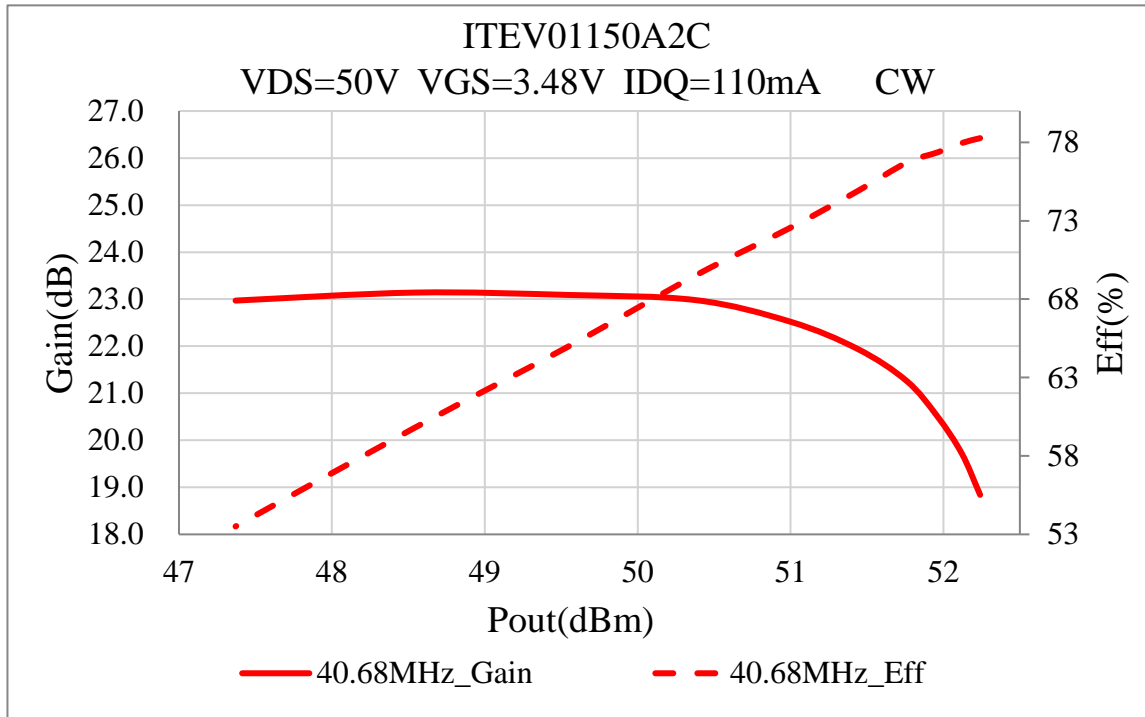
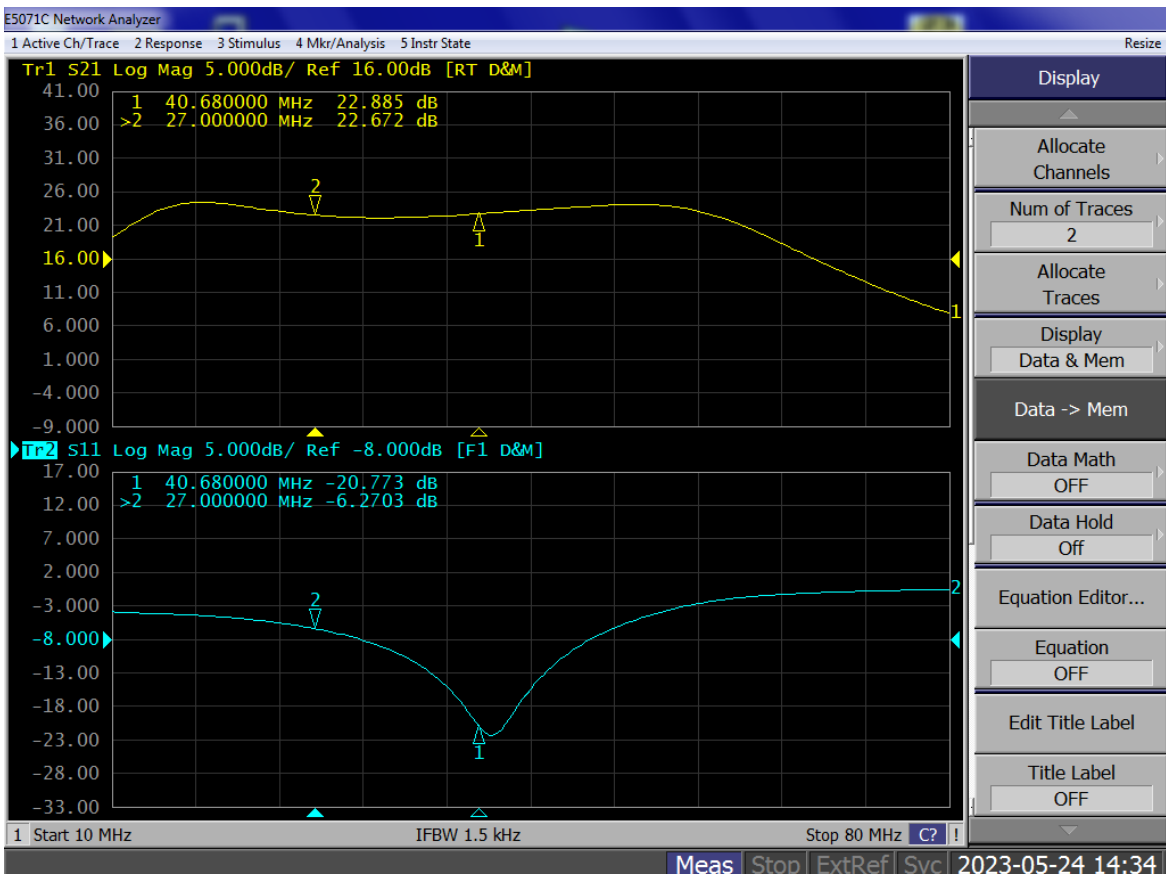


Figure 2: Network analyzer output S11/221



Reference Circuit of Test Fixture Assembly Diagram

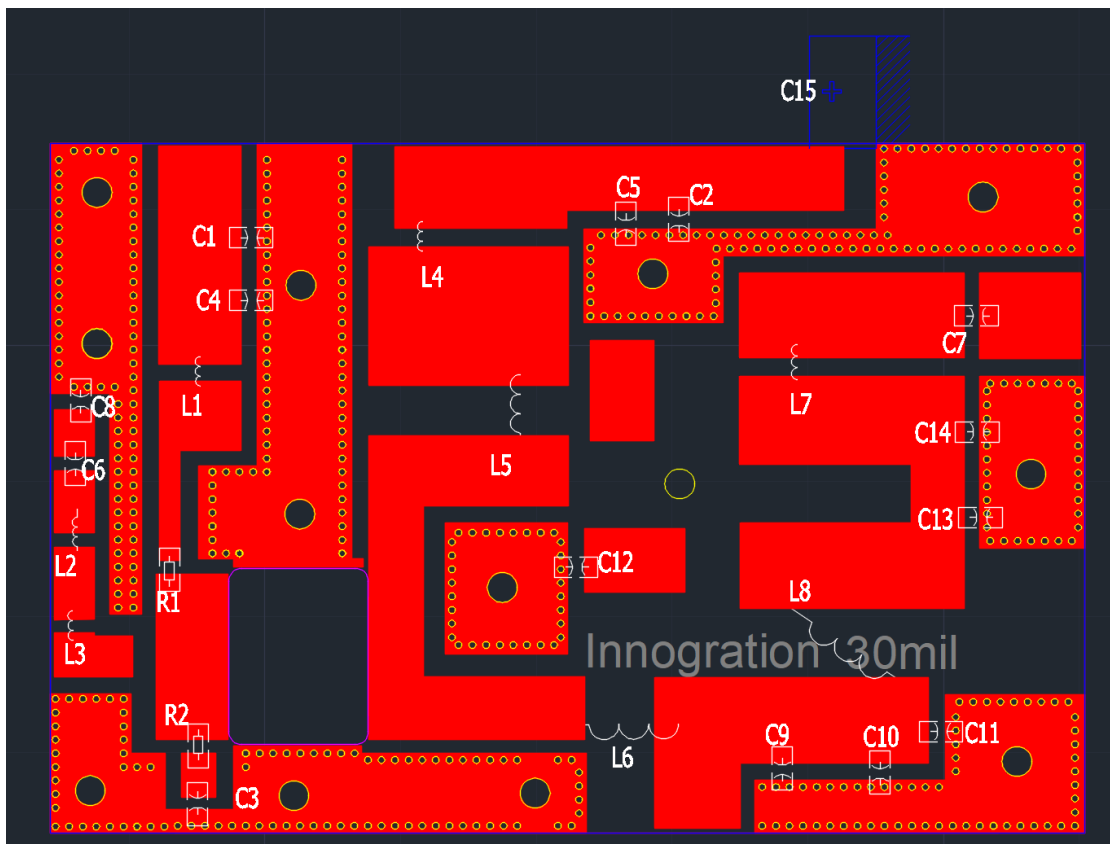
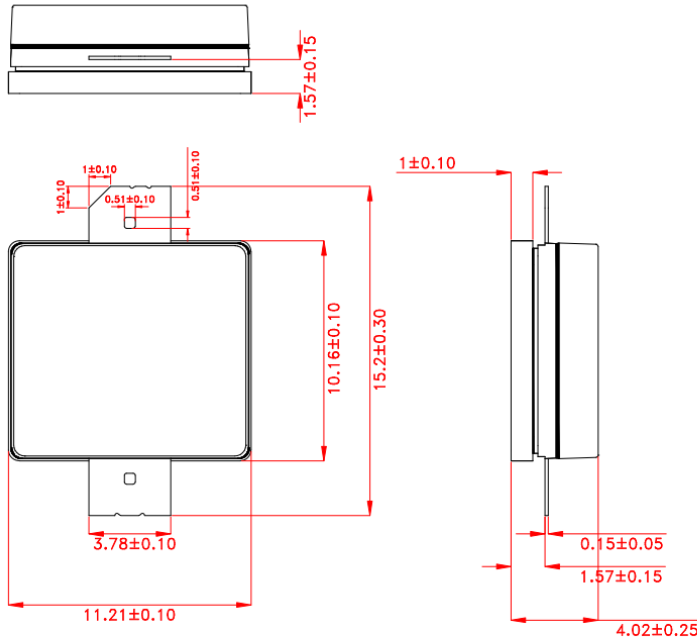


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1,C2,C3,	10uF 100V	Ceramic multilayer capacitor
C4,C5,C6,C7	10nF 100V	Ceramic multilayer capacitor
C14	470uF,63V	Electrolytic Capacitor
C15	150pF	MQ101111
C8	20pF	MQ101111
C9,C10	33pF	MQ101111
C11	56pF	MQ101111
C12	68pF	MQ101111
C13	82pF	MQ101111
L1	47nH	
L6	150nH	
R1	300 Ω , 1206	Chip Resistor
R2	10 Ω	Chip Resistor
L2	1.5m, 14 turns	
L3,L5	1.5m, 4turns	
L4	1.5m, 3turns	
PCB	30Mil Rogers4350	

Package Dimensions (Unit:mm)



Unit:mm

Tolerance ±0.10mm, Except as Noted.

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/8/27	Rev 1.0	Preliminary Datasheet Creation from C9 version to A2C

Application data based on SYX-24-29

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