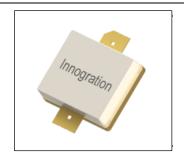
300W, 50V High Power RF LDMOS FETs

Description

designed for wide-band commercial and industrial applications with frequencies HF to 500MHz, in new generation highly cost effective open cavity package.

It is featured by single ended configuration for high power and high ruggedness, suitable for Industrial, Scientific and Medical application

The ITEV01150A2C is a 300-watt capable, high performance, unmatched LDMOS FET,



Typical performance(on Innogration test board with device soldered)
 Signal: CW, Vgs=3.2V,Vds=50V,Idq=100mA

Freq	Pin	Pout	Pout	lds	Gain	Eff	2 nd harmonic
(MHz)	(dBm)	(dBm)	(W)	(A)	(dB)	(%)	(dBc)
40.68	35	55	316	7.9	20	80	-20

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- · Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
DrainSource Voltage	$V_{\scriptscriptstyle DSS}$	+135	Vdc
GateSource Voltage	$V_{\sf GS}$	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	TJ	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	Doug	0.55	00/14/
T _C = 85°C, T _J =200°C, DC test	RθJC	0.55	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22A114)	Class 2

Document Number: ITEV01300A2C Preliminary Datasheet V1.0

Table 4. Electrical Characteristics ($T_A = 25$ °C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage	V		125		V
V_{GS} =0, I_{DS} =1.0mA	$V_{(BR)DSS}$		135		v
Zero Gate Voltage Drain Leakage Current				1	^
$(V_{DS} = 75V, V_{GS} = 0 V)$	I _{DSS}			I	μΑ
Zero Gate Voltage Drain Leakage Current				1	μΑ
$(V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V})$	I _{DSS}				
GateSource Leakage Current				1	٨
$(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$	I_{GSS}			1	μΑ
Gate Threshold Voltage	M. (ii)		0.05		V
$(V_{DS} = 50V, I_D = 600 \mu A)$	V _{GS} (th)		2.65		V
Gate Quiescent Voltage			2.2		\/
$(V_{DD} = 50 \text{ V}, I_D = 100 \text{ mA}, \text{Measured in Functional Test})$	$V_{GS(Q)}$		3.2		V

 $\textbf{Load Mismatch (In Innogration Test Fixture, 50 ohm system):} \ V_{DD} = 50 \ Vdc, \ I_{DQ} = 100 \ mA, \ f = 100 \ mHz, \ pulse \ width: 100 us, \ duty \ cycle: 10\% \ make the pulse \ width: 100 us, \ duty \ dut$

Load 65:1 All phase angles, at 300W Pulsed CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

Figure 1: CW Gain and Power Efficiency as a Function of Pout at 40.68MHz

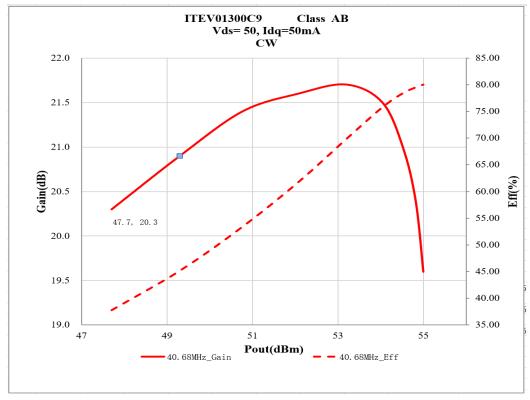
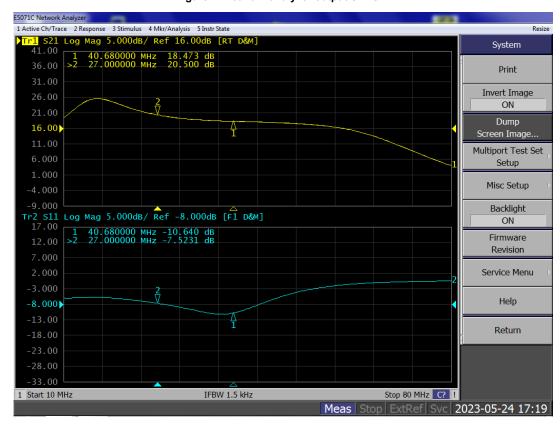


Figure 2: Network analyzer output S11/S21



Reference Circuit of Test Fixture Assembly Diagram

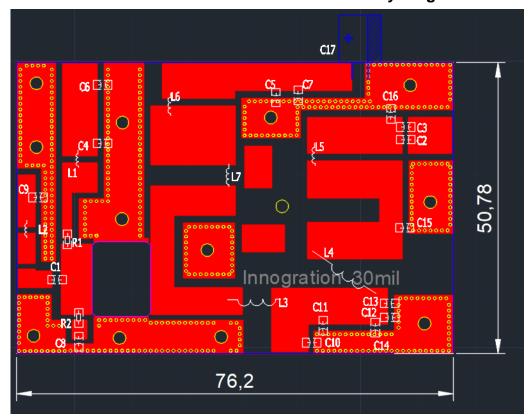
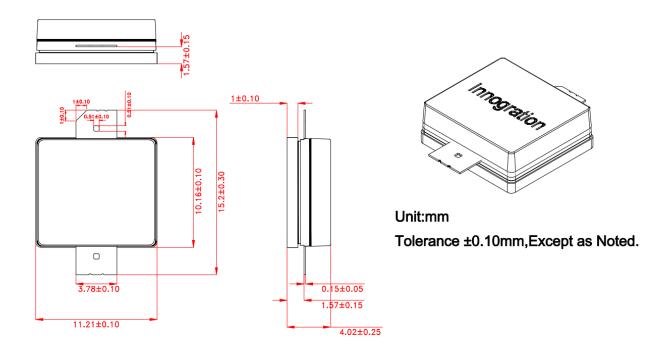


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggestion	
C1,C2,C3,	10uF 100V	Ceramic multilayer capacitor	
C4,C5,C6,C7,C16	10nF 100V	Ceramic multilayer capacitor	
C14	470uF,63V	Electrolytic Capacitor	
C15	200pF	MQ101111	
C8	100pF	MQ101111	
C9,C11	33pF	MQ101111	
C10	22pF	MQ101111	
C12	150pF	MQ101111	
C13	56pF	MQ101111	
C15	39pF	MQ101111	
L1	47nH		
L6	150nH		
R1	300 Ω , 1206	Chip Resistor	
R2	5 Ω	Chip Resistor	
L2,L7	1.5mm,6 turns, φ 5		
L3	1.5mm,2 turns,		
L4	1.5mm,4 turns, ∳5		
PCB	30Mil Rogers4350		

Package Dimensions (Unit:mm)



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/8/27	Rev 1.0	Preliminary Datasheet Creation from C9 version to A2C

Application data based on SYX-24-28

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