30W, 28V High Power RF LDMOS FETs

ITEH16030J2

Description

The ITEH16030J2 is a 30-watt, unmatched LDMOS FETs, designed for multiple applications with frequencies from VHF to 1600 MHz.

It can be used in Class AB/B and Class C to support CW,Pulsed CW or any modulation Signal.

•Typical Performance (On Innogration fixture with device soldered) in different bands

VDD = 28 Volts, , Idq=150mA CW

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
650	44.32	27.04	58.97	22.14	45.46	35.15	65.41
700	44.55	28.49	61.09	21.89	45.60	36.32	67.36
750	44.44	27.77	61.90	22.21	45.66	36.82	69.10
800	44.01	25.20	61.56	22.29	45.35	34.27	69.63
850	43.64	23.12	62.35	22.20	44.98	31.47	70.37

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1080	43.87	24.38	60.77	18.34	44.92	31.08	64.82
1150	44.34	27.14	57.21	17.68	45.43	34.91	61.32
1200	44.56	28.55	57.16	17.55	45.59	36.20	61.09
1250	44.57	28.66	57.66	17.98	45.61	36.38	61.78
1300	44.38	27.42	59.08	17.63	45.38	34.54	63.07
1340	44.02	25.24	60.00	17.78	45.01	31.71	63.93

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	1.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=0V; I_{DS}=1mA	V_{DSS}	65			V
Zero Gate Voltage Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}			1	μA
Gate--Source Leakage Current	V_{GS} = 9 V, V_{DS} = 0 V	I_{GSS}			1	μA
Gate Threshold Voltage	V_{DS} = 28V, I_D = 300 μA	$V_{GS(th)}$		1.75		V
Gate Quiescent Voltage	V_{DS} = 28 V, I_{DS} = 200 mA, Measured in Functional Test	$V_{GS(Q)}$		2.7		V

650-850MHz application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

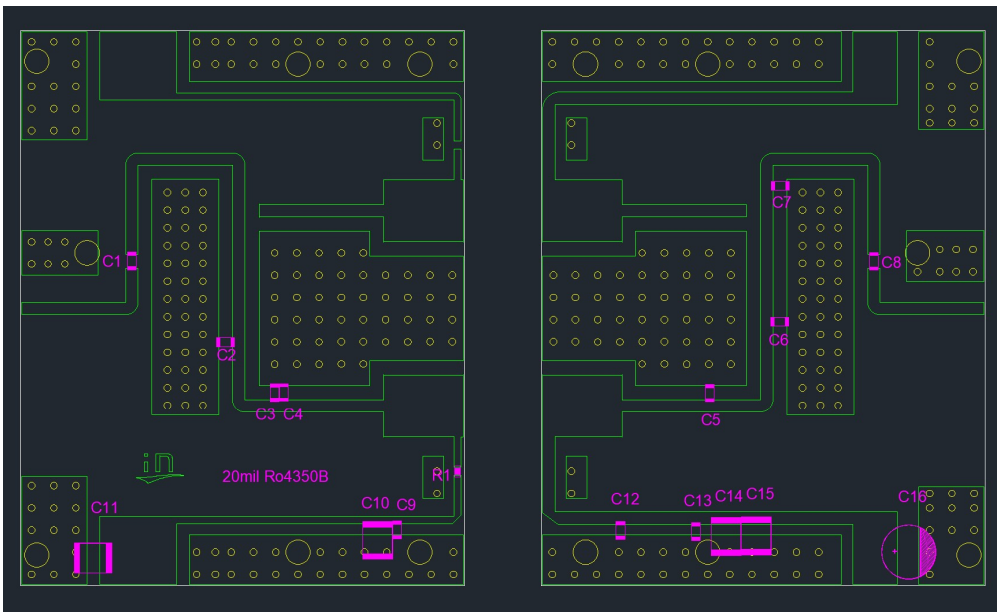


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1	0603	20pF	1
C2	0603	3pF	1
C3	0603	2pF	1
C4	0603	8.2pF	1
C5	0805	7.5pF	1
C6	0603	2.4pF	1
C7	0603	1.1pF	1
C8,C9,C12,C13	0603	68pF	4
R1	0603	10ohm	1
C10,C11,C14,C15	1210	10uF/63V	4
C16	\	470uF/63V	1
U1	J2E	ITEH16030J2	1

TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Output at Idq =150mA

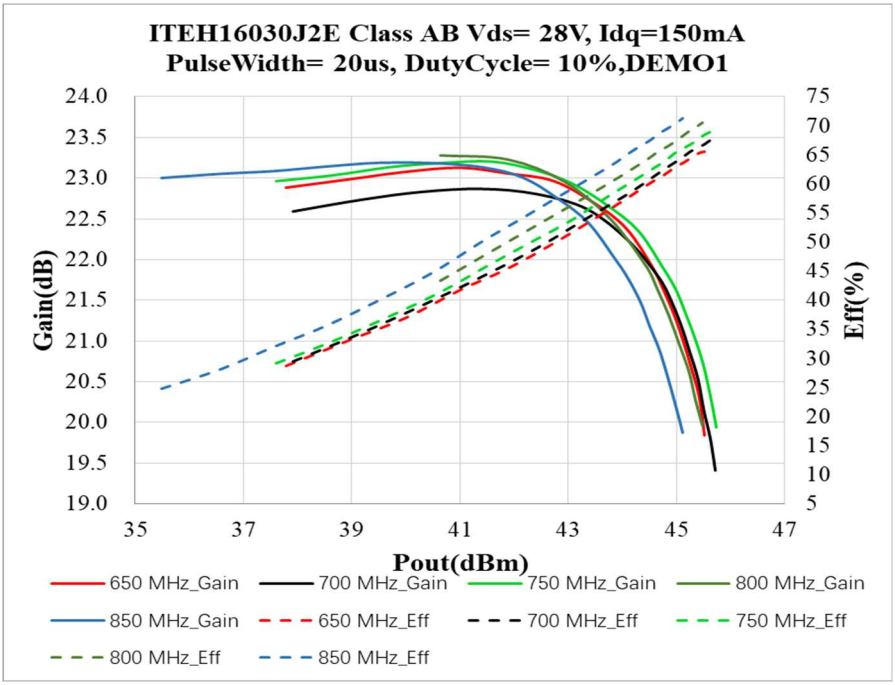
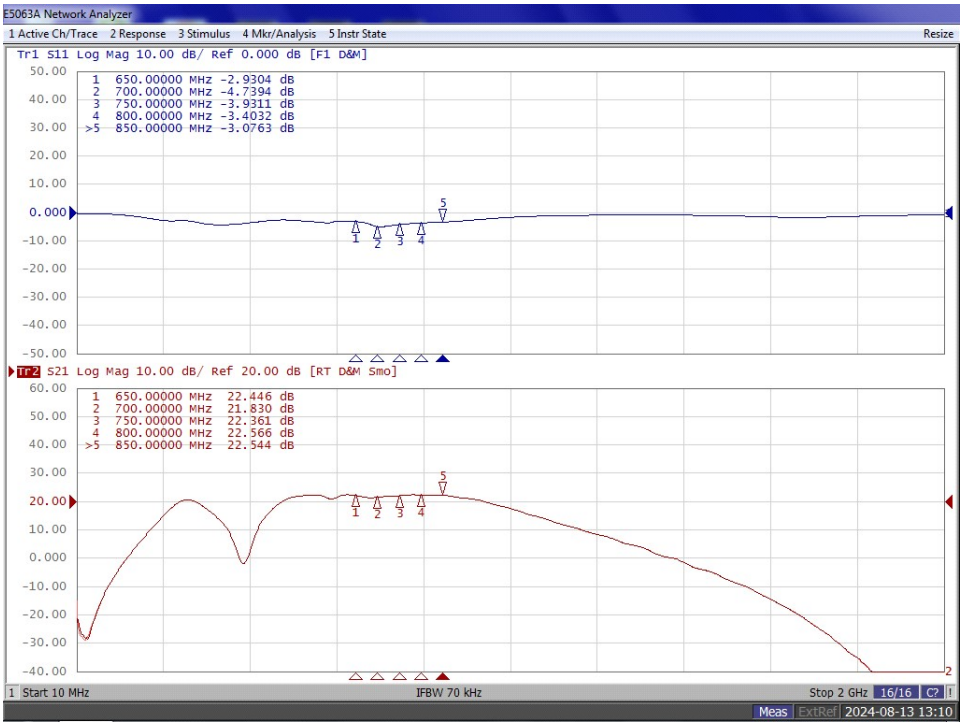


Figure 4.Network analyzer output S11/S21



1.03-1.34GHz application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

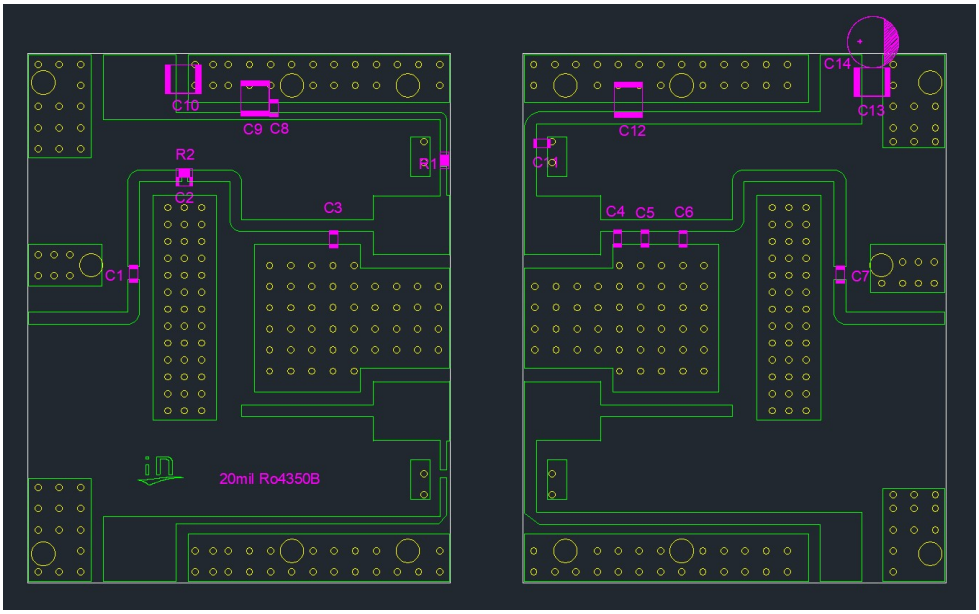


Figure 6. Test Circuit Component Layout

Table 6. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1	0603	8.2pF	1
C2,C7,C8,C11	0603	20pF	4
C3	0603	5.6pF	1
C4	0603	3.3pF	1
C5	0805	3pF	1
C6	0603	1.2pF	1
R1	0603	10ohm	1
R2	0603	50ohm	1
C9,C10,C12,C13	1210	10uF/63V	4
C14	\	470uF/63V	1
U1	J2E	ITEH16030J2	1

TYPICAL CHARACTERISTICS

Figure 7. Power Gain and Drain Efficiency as function of Power Output at Idq =20mA

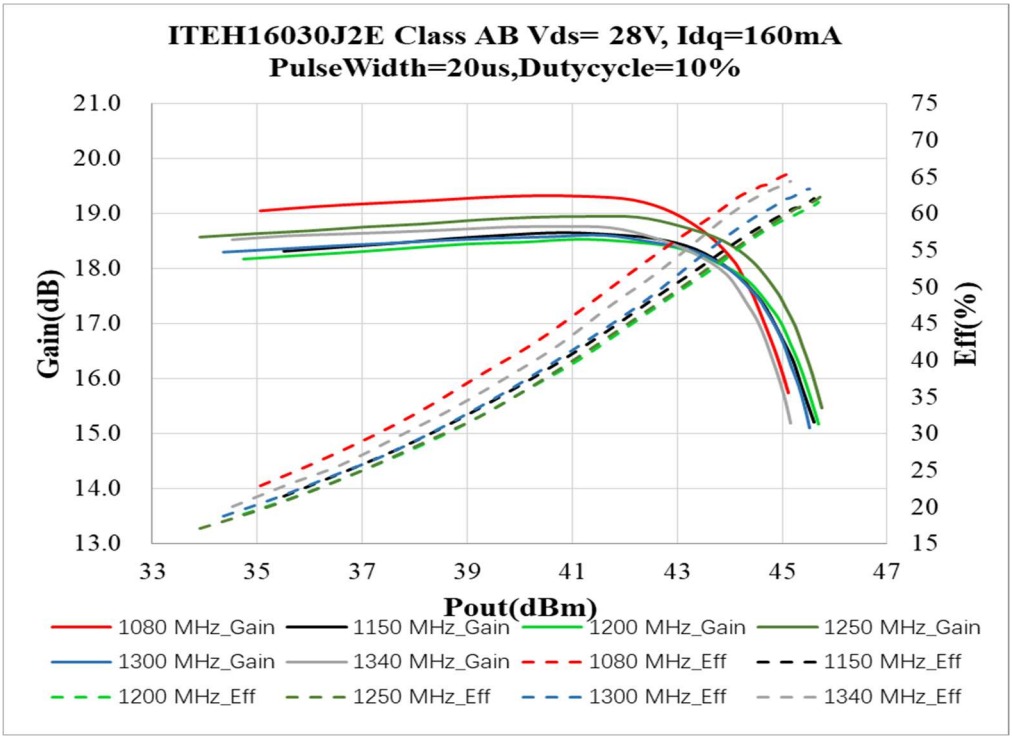
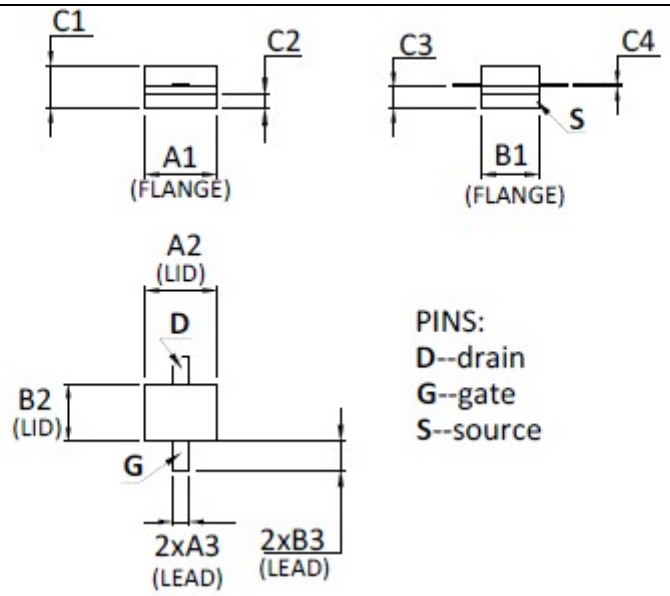


Figure 8.Network analyzer output S11/S21

Package Outline

Earless ceramic package; 2 leads



DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX
A1	0.195	0.205	4.953	5.207
A2	0.195	0.205	4.953	5.207
A3	0.042	0.052	1.070	1.330
B1	0.155	0.165	3.937	4.191
B2	0.155	0.165	3.937	4.191
B3	0.060	0.100	1.524	2.540
C1	0.110	0.130	2.794	3.302
C2	0.034	0.044	0.870	1.130
C3	0.057	0.067	1.447	1.700
C4	0.004	0.006	0.101	0.150

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-MMS					12/13/2017

Figure 1. Package Outline PKG-MMS

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/8/16	Rev 1.0	Product Datasheet

Application data based on CWZ-24-21/22

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