



## 2.4-2.5GHz, 100W, High Power RF LDMOS FETs

### Description

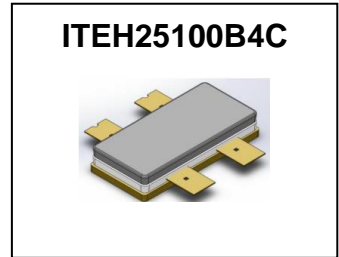
The ITEH25100B4C is a dual path (A+B) 100W, internally matched LDMOS FETs, designed for multiple use especially RF Energy application including cooking, heating and medical with frequencies from 2400 to 2500MHz.

**It is the low cost version of its ceramic peer: ITCH25100B4.**

• Typical CW Performance (on Innegration fixture with device soldered)

$V_{ds}=28V$ ,  $V_{gs}=2V$

Freq (MHz)	Pin (dBm)	Pout (W)	Id (A)	Eff (%)
2400	40	123	7.97	55
2450	40	128	8.29	55
2500	40	112	7.25	55



### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

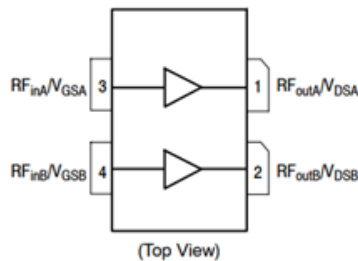


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	65	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+32	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_j$	+225	°C



**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T <sub>case</sub> = 85°C, T <sub>j</sub> = 200°C, DC Power supply	R <sub>θJC</sub>	0.5	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

**Table 4. Electrical Characteristics of each path: A or B (TA = 25 °C unless otherwise noted)**

Characteristic	Symbol	Min	Typ	Max	Unit
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**DC Characteristics**

Drain-Source Breakdown Voltage (V <sub>GS</sub> =0V; I <sub>D</sub> =100uA)	V <sub>DSS</sub>	65	---	---	V
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 28 V, V <sub>GS</sub> = 0 V)	I <sub>DSS</sub>	---	---	10	μA
Gate--Source Leakage Current (V <sub>GS</sub> = 6 V, V <sub>DS</sub> = 0 V)	I <sub>GSS</sub>	---	---	1	μA
Gate Threshold Voltage (V <sub>DS</sub> = 28V, I <sub>D</sub> = 600 uA)	V <sub>GS(th)</sub>	---	1.75	---	V
Gate Quiescent Voltage (V <sub>DD</sub> = 28V, I <sub>DQ</sub> = 100 mA, Measured in Functional Test)	V <sub>GS(Q)</sub>		2.4		V

**Load Mismatch (In Innegration Test Fixture, 50 ohm system) of of each path: A or B:** V<sub>DD</sub> = 28 Vdc, I<sub>DQ</sub> =5 mA, f = 2450MHz

VSWR 10:1 at 50W pulse CW Output Power	No Device Degradation
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**Figure 2 Efficiency and power gain as function of Pout**

Signal: Pulse width 100us, duty cycle 10% , Vgs= 2.24V, Vdd= 28V, Idq=5mA

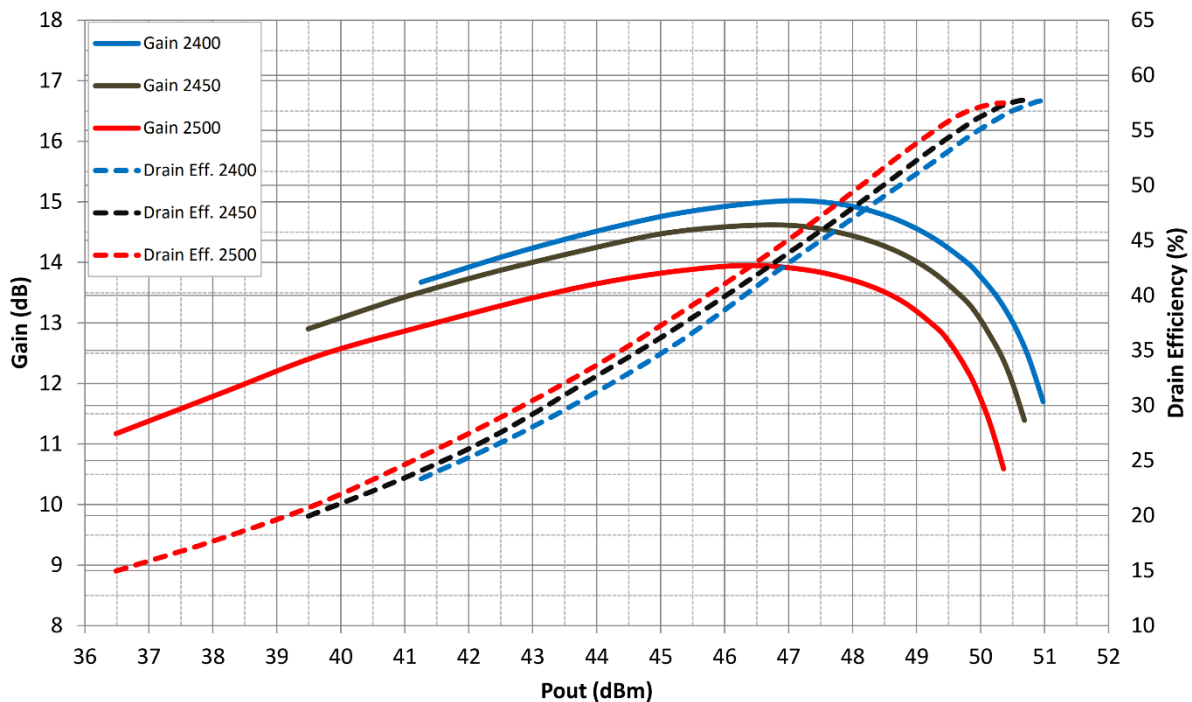


Figure 3: Network analyzer output, S11 and S21

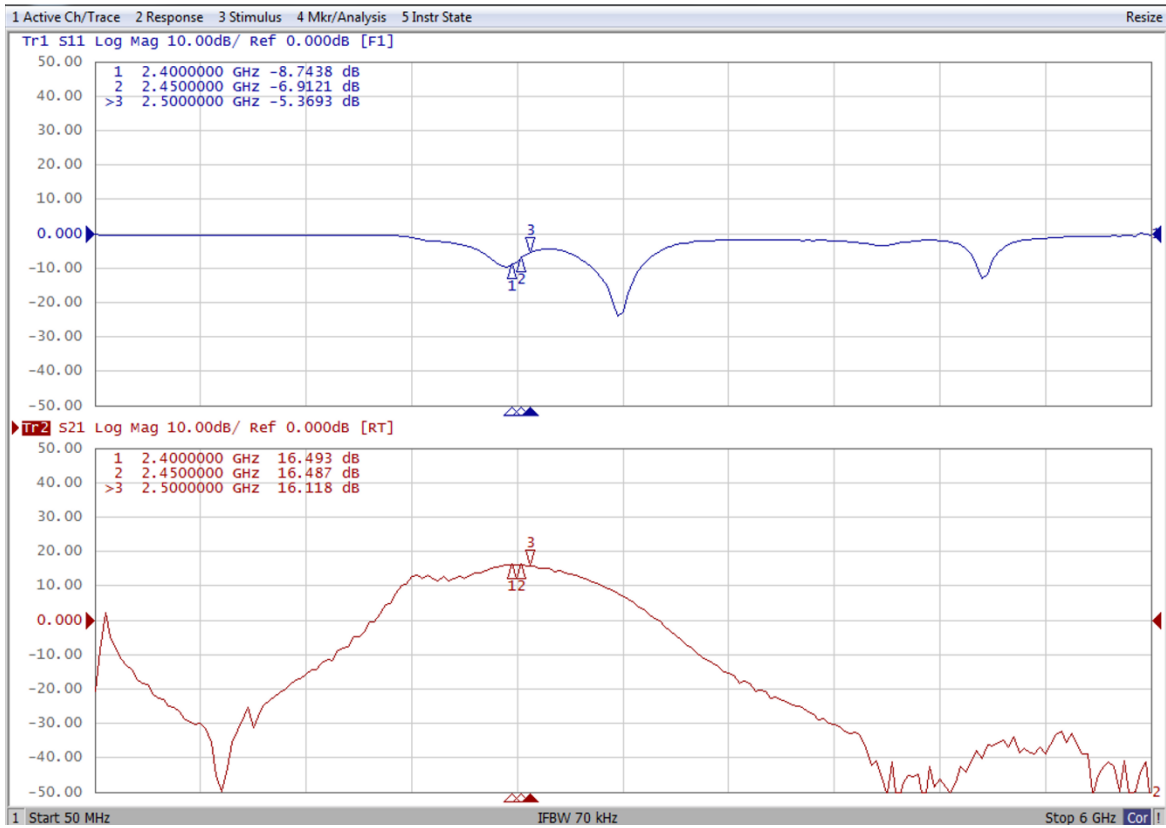


Figure 4: Layout picture (original Gerber file upon request)

Board material: Ro 4350B, Er = 3.48, thickness 20 mils, 1oz copper, unit mm ,

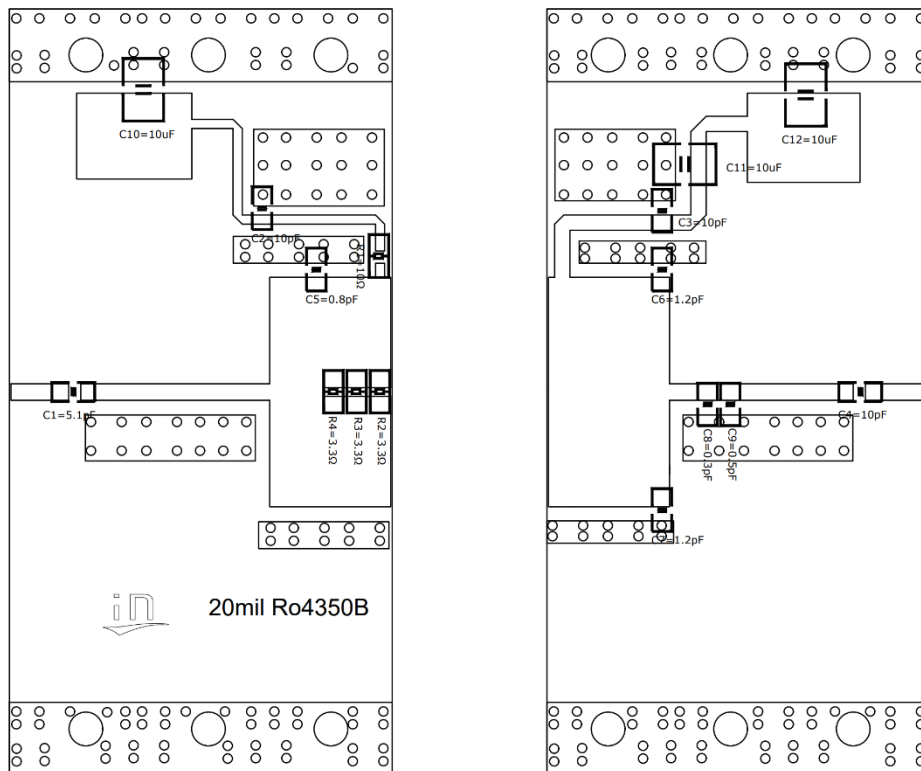




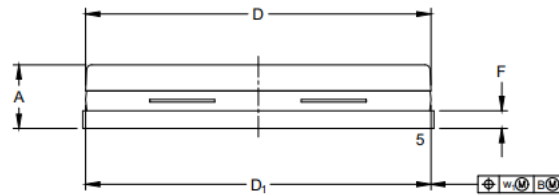
Table 5. List of components

Reference	Footprint	Value	Quantity
C2, C3, C4	0603	10pF/250V	3
C1	0603	5.1pF/250V	1
C5	0603	0.8pF/250V	1
C6, C7	0603	1.2pF/250V	2
C8	0603	0.3pF/250V	1
C9	0603	0.5pF/250V	1
C10, C11, C12	1210	10uF/100V	3
R1	0603	10R	1
R2, R3, R4	0603	3.3R	3
/	B4C	ITEH25100B4C	1

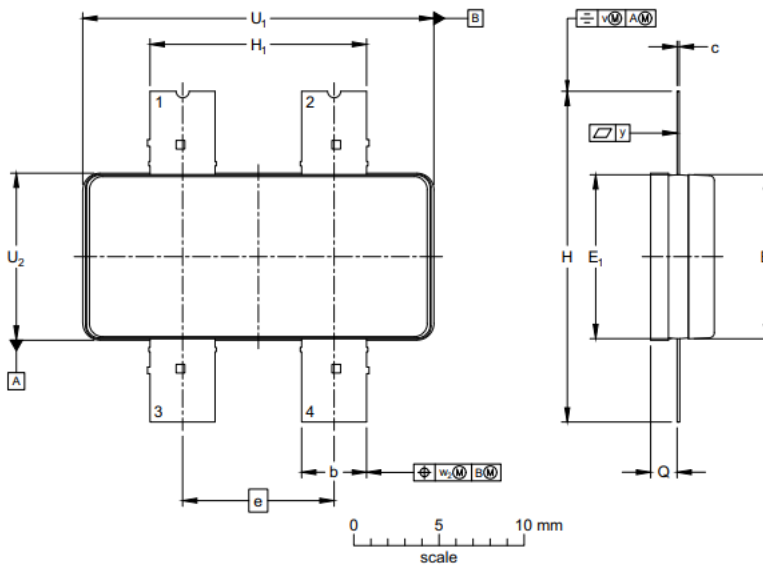


## Package Outline

### Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5



Dimensions

Unit	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	e	F	H	H <sub>1</sub>	Q <sup>(1)</sup>	U <sub>1</sub>	U <sub>2</sub>	v	w <sub>1</sub>	w <sub>2</sub>	y
mm	max 4.01	3.91	0.18	20.42	20.37	9.80	9.75		1.14	19.53	12.83	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom							8.89										
	min 3.40	3.71	0.13	20.12	20.17	9.50	9.55		0.94	19.33	12.57	1.45	20.50	9.70				

## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/5/11	V1	Preliminary Datasheet Creation based on Path A 50W data
2024/7/4	V1.1	Add 100W data as Path A+B

Application data based on ZBB-23-23/24-21

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