



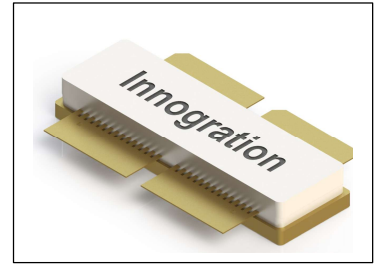
1400W, 28V High Power RF LDMOS FETs

Description

The ITGH09400D4C is a 400W capable, internally matched, push pull, 28V LDMOS designed for multiple application up to 1GHz, especially ISM and RF Energy at 915/433MHz etc
It can be configured as Class AB or Class C for CW or pulsed CW

• Typical 915MHz CW Performance (on Innogrations fixture with device soldered)

V_{ds}=28V, V_{gs}=2V



Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
915	55.79	379.7	71.1	18.74	56.35	431.3	72.4

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	65	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+28	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _{case} = 25°C, DC Power supply	R _{θJC}	0.25	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Breakdown Voltage (V _{GS} =0V; I _D =100uA)	V _{DSS}	65	---	---	V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 V, V _{GS} = 0 V)	I _{DSS}	---	---	10	μA



Gate--Source Leakage Current ($V_{GS} = 6\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}	-----	-----	1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{ V}$, $I_D = 600\text{ uA}$)	$V_{GS(th)}$	-----	1.75	-----	V
Gate Quiescent Voltage ($V_{DD} = 28\text{ V}$, $I_{DQ} = 100\text{ mA}$, Measured in Functional Test)	$V_{GS(Q)}$		2.2		V

Load Mismatch (In Innegration Test Fixture, 50 ohm system): $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 100\text{ mA}$, $f = 915\text{ MHz}$

VSWR 10:1 at 400W pulse CW Output Power	No Device Degradation
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915MHz

Figure 1 Efficiency and power gain as function of Pout at Vds=28V

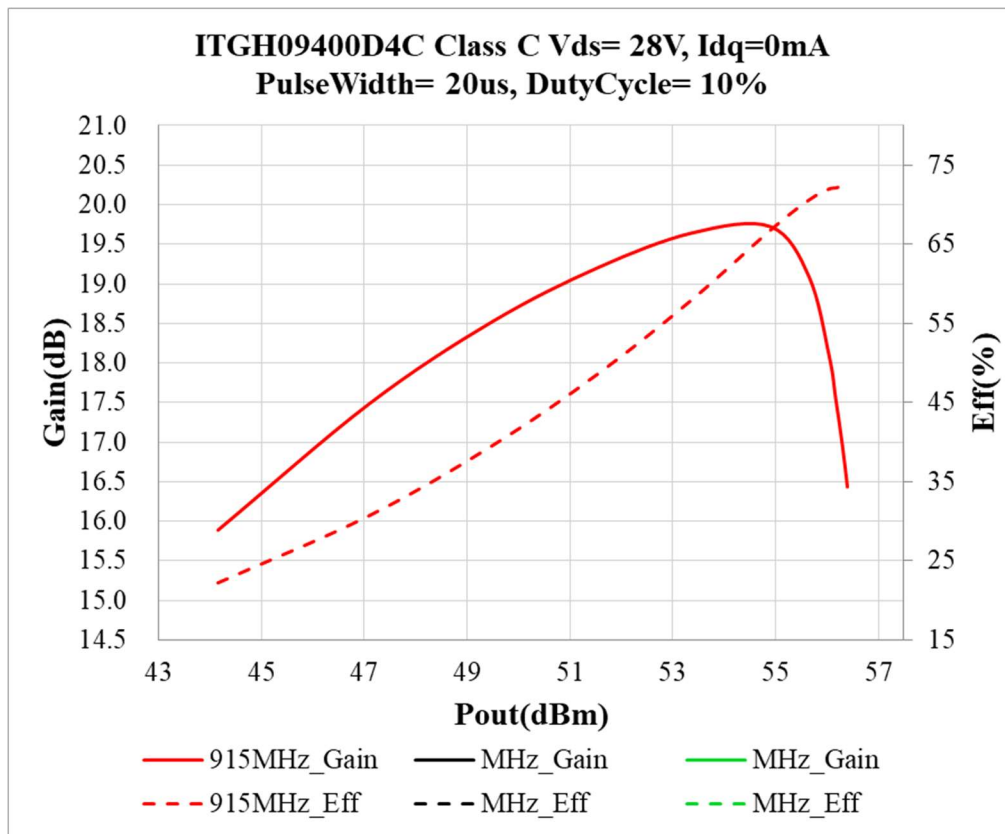


Figure 2: Network analyzer output, S11 and S21



Figure 3: Layout picture (original Gerber file upon request)

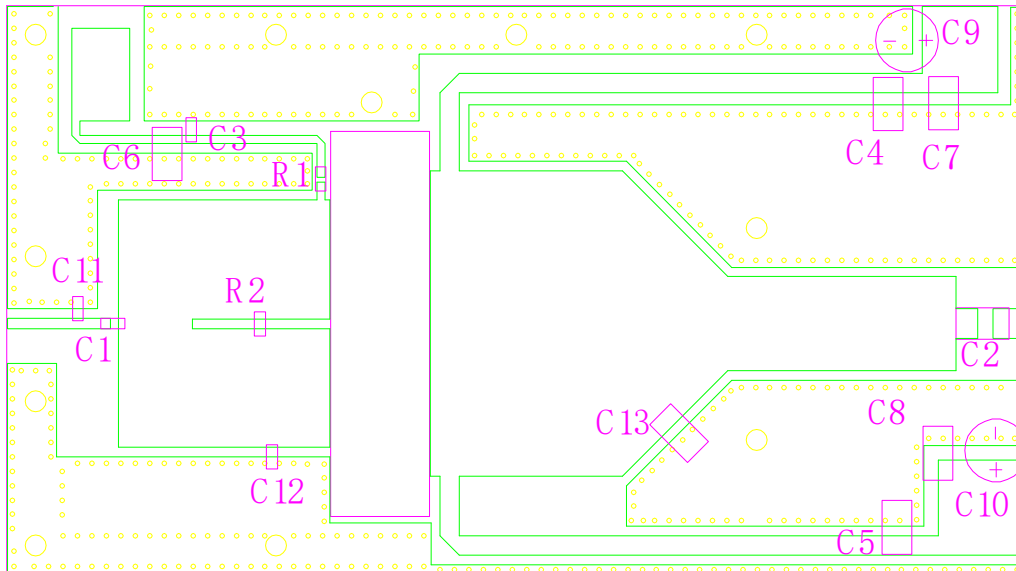


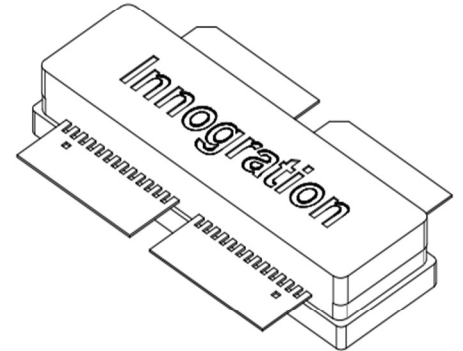
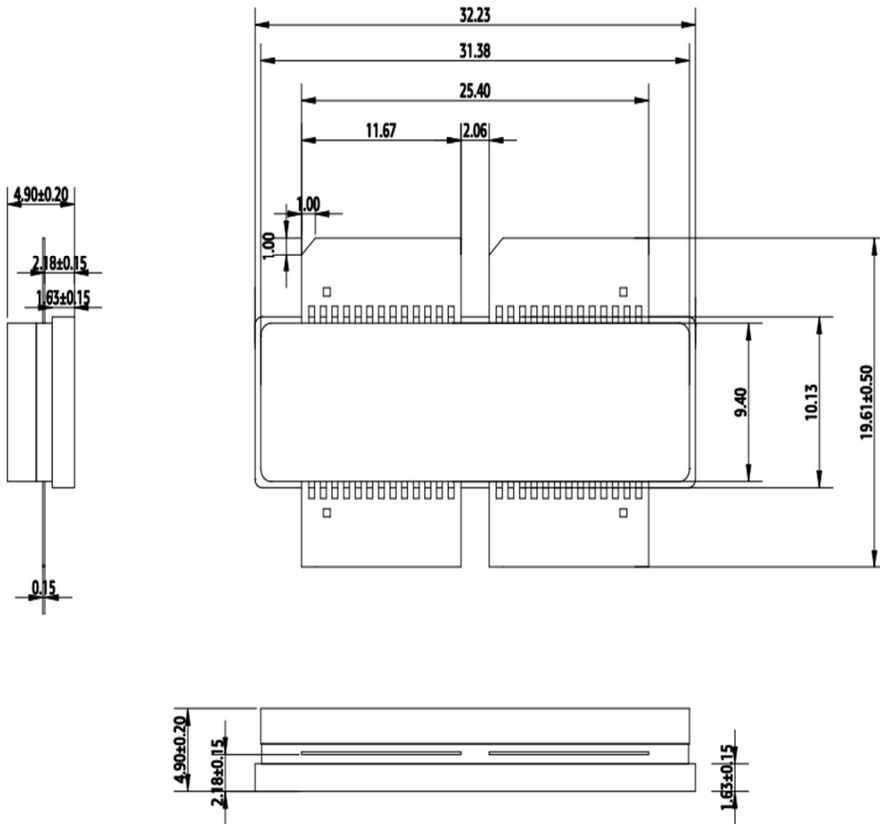


Table 5. List of components

Designator	Footprint	Comment	Quantity
C1, C3	0603/0805	47 pF	2
C2, C4, C5	1210	47 pF	3
C4, C5	1210	47pF	2
C6, C7, C8	1210	10uF/100V	3
C9, C10		1000uF/63V	2
C11	0603/0805	15 pF	1
C11, C12	0603/0805	10 pF	2
C13	1210	6.8 pF	1
R1, R2	0603/0805	10Ω	2



Earless Flanged Plastic Air Cavity Package; 4 leads



Unit:mm
Tolerance ±0.10mm, Except as Noted.

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/7/15	V1	Preliminary Datasheet Creation

Application data based on LSM-24-24

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