600W, 50V High Power RF LDMOS FETs

Description

The ITEV01600B4C is a 600-watt capable, high performance, unmatched LDMOS FET, designed for HF/VHF. It can be used for both CW and pulse application.

It is featured for high power and high ruggedness, low cost, suitable for ISM RF Energy application.



• Typical Performance (On Innogration 13.56MHz fixture with device soldered):

ITEV01600B4C VGS=3.36V VDS=50V IDQ=200mA CW						
Freq(MHz)	Pout(dBm)	Pout(W)	IDS(A)	Pin(dBm)	Gain(dB)	Eff(%)
13.56	58.07	641.2	16.38	42	16.07	78.29
13.56	57.86	610.9	15.96	41	16.86	76.56
13.56	57.63	579.4	15.54	40	17.63	74.57
13.56	57.38	547.0	15.09	39	18.38	72.50
13.56	57.11	514.0	14.67	38	19.11	70.08
13.56	56.82	480.8	14.21	36.99	19.83	67.68
13.56	56.45	441.6	13.68	35.98	20.47	64.56
13.56	56.01	399.0	13.09	34.99	21.02	60.97

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- On chip RC network enable high stability and ruggedness
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
DrainSource Voltage	V _{DSS}	135	Vdc
GateSource Voltage	V _{GS}	-7 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	T₃	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature	Do 10	0.4	°C/W
80°C, 600W CW, 50 Vdc, IDQ = 200 mA	Rejc	0.4	
Transient thermal impedance from junction to case	7th	0.08	°C/W
Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	0.08	

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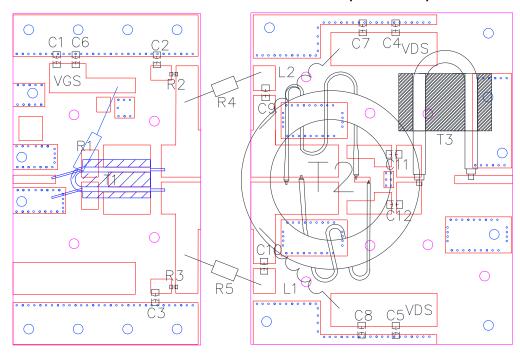
Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

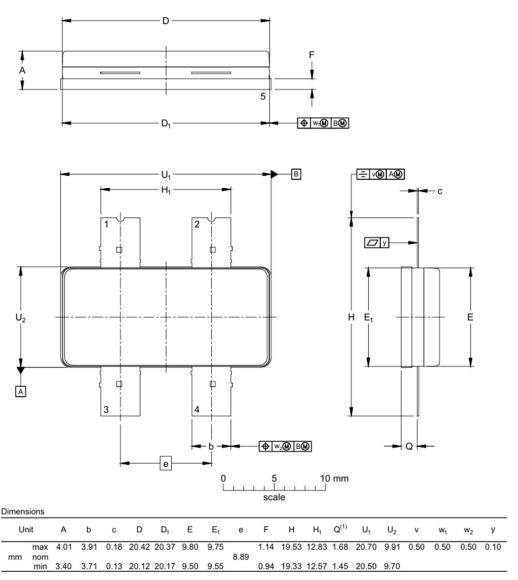
Characteristic		Min	Тур	Max	Unit
C Characteristics (Per Side)					
Drain-Source Voltage	V	120			V
V _{GS} =0, I _{DS} =18.0mA	V _{(BR)DSS} 130				V
Zero Gate Voltage Drain Leakage Current				1	
$(V_{DS} = 50V, V_{GS} = 0 V)$	I _{DSS}			Į.	μΑ
Gate—Source Leakage Current				1	
$(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$	I_{GSS}			1	μΑ
Gate Threshold Voltage	V (#5)		2.6		V
$(V_{DS} = 50V, I_D = 600 \mu A)$	V _{GS} (th)		2.0		V
Gate Quiescent Voltage	V		3.36		V
(V _{DD} = 50 V, I _D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.30		V
Common Source Input Capacitance	C _{ISS}		200		pF
(V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz) Each section side of device					
measured					
Common Source Output Capacitance	Coss		50		pF
$(V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz)$ Each section side of device					
measured					
Common Source Feedback Capacitance	C _{RSS}		1		pF
(V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz) Each section side of device					
measured					

Reference Circuit of Test Fixture (13.56MHz)



Component	Description	Suggestion
C1~C5	10uF Ceramic multilayer capacitor	
C6~C12	Ceramic multilayer capacitor, 10nF	
R1	300 Ω	
R2,R3	10 Ω	
R4,R5	200 Ω	
L1,L2	T68-2,12turns 1.5mm	
Т1	4:1 No43, d=1mm	
T2	4:1 No.43 12.5ohm coaxial, 300mm	SFF-12.5-1.5
Т3	25ohm No.43 150mm	SFF-25-1.5
PCB	0.762mm [0.030"] thick, εr=3.48, Rogers RO4350B, 1 oz. copper	

Earless Flanged Plastic Air Cavity Package; 4 leads



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/3/28	Rev 1.0	Preliminary Datasheet ,migrated from B4 to B4C

Application data based on HL-23-05/LBG-24-12

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