



GaN 50V, 1200W, 915MHz RF Power Transistor

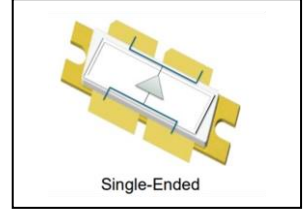
STBV101K5RD4

Description

The STBV101K5RD4 is a 1200W capable, single ended, internally matched GaN HEMT, ideal for ISM or RF energy applications at 915MHz

There is no guarantee of performance when this part is used outside of stated frequencies.

Please notice that both leads at input and output side are internally connected, to configure this device as single ended ,shown as right picture.



It is recommended to operate this device around 1000W CW

- Typical RF performance at 915MHz applications

V_{ds}=50V, V_{gs}=-4.2V, T_c=25 degree C

Pulsed CW: 20us, 10% duty cycle,

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
915	59.8	955.3	75.0	17.85	60.87	1221.5	81.4

CW

Freq (MHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Ids (A)	Gain (dB)	Eff (%)
915	42.3	60.01	1000	27.70	17.7	75.21
915	44.3	60.68	1170	31.20	16.4	78.13

Recommended driver: ITGV20040J2 (50V LDMOS)

Applications

- 915MHz RF Energy
- P band power amplifier
- Avionics Power Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+200	Vdc
Gate--Source Voltage	V _{GS}	-8 to +0.5	Vdc
Operating Voltage	V _{DD}	55	Vdc
Maximum gate current	I _{gs}	198	mA
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
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Thermal Resistance, Junction to Case by FEA T _c = 25°C, at Pd=350W	R _{θJC}	0.3	°C /W
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Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

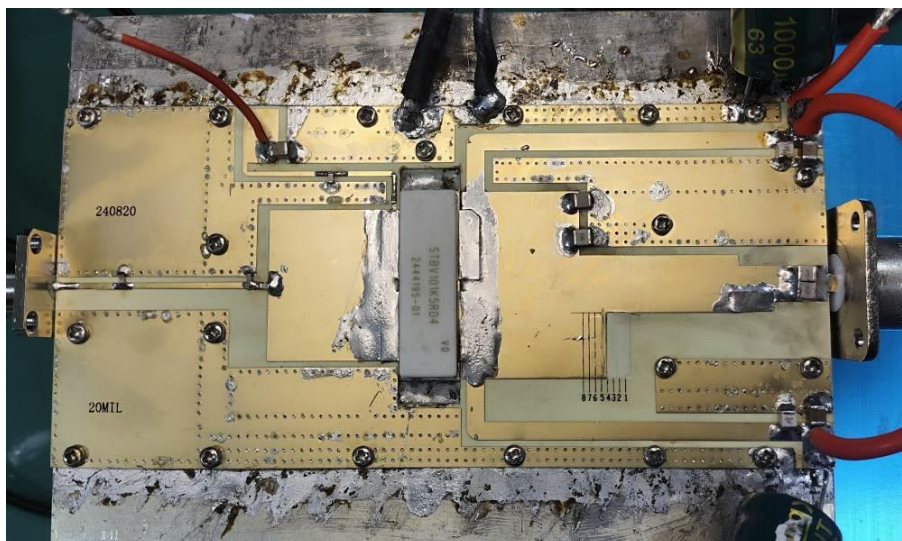
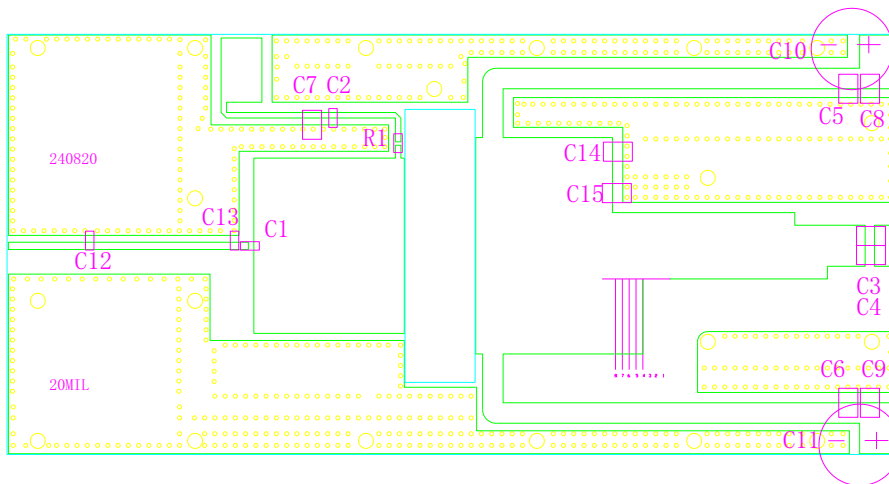
DC Characteristics (measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{GS} =-8V; I _{DS} =198mA	V _{DSS}		200		V
Gate Threshold Voltage	V _{DS} =10V, I _D =198mA	V _{GS(th)}	-4	-	-2	V
Gate Quiescent Voltage	V _{DS} =50V, I _{DS} =500mA, Measured in Functional Test	V _{GS(Q)}		-3.3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	915MHz, P _{out} =1000W pulse CW All phase, No device damages	VSWR		10:1		

Reference Circuit of Test Fixture Assembly Diagram
DXF file upon request





Designator	Footprint	Comment	Quantity
C1, C2	0603/0805	47pF	2
C3, C4	1210	27pF	2
C5, C6	1210	47pF	2
C7, C8, C9	1210	10uF/100V	5
C11, C11		1000uF/63V	2
C12	0603/0805	3.0 pF	1
C13	0603/0805	12 pF	1
C14	1210	4.3 pF	1
C15	1210	8.2 pF	1
R1	0603	10 Ω	1

TYPICAL CHARACTERISTICS

Figure 2: S11/S21 output from Network analyser (VDS= 50V, IDQ=500 mA Vgs =-3.3V)

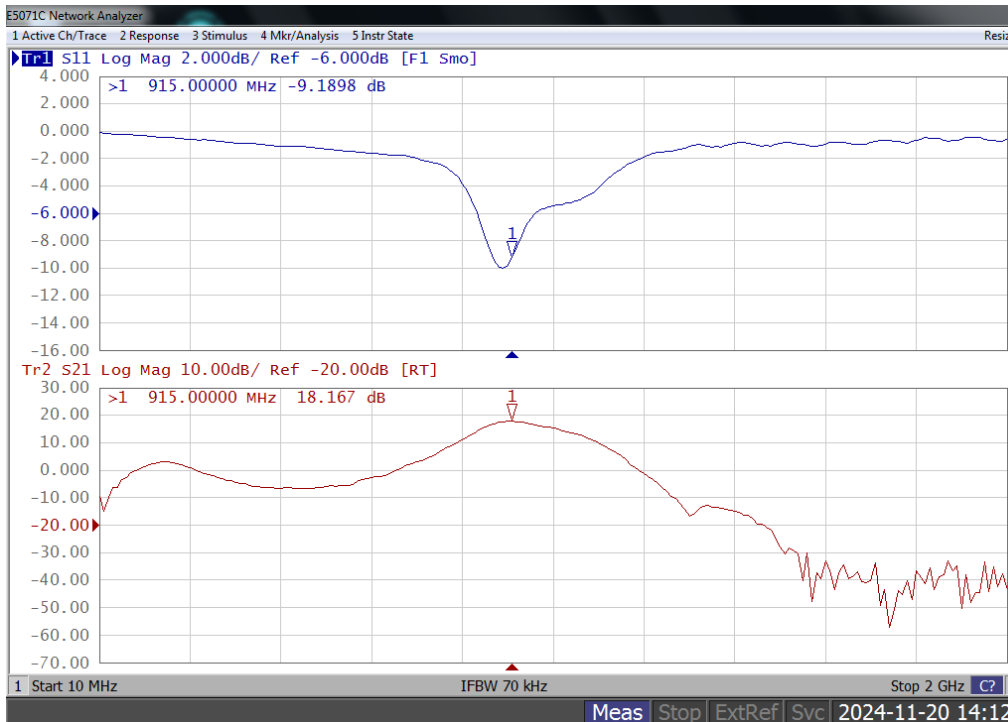


Figure 3: Power gain, Eff as function of Pout

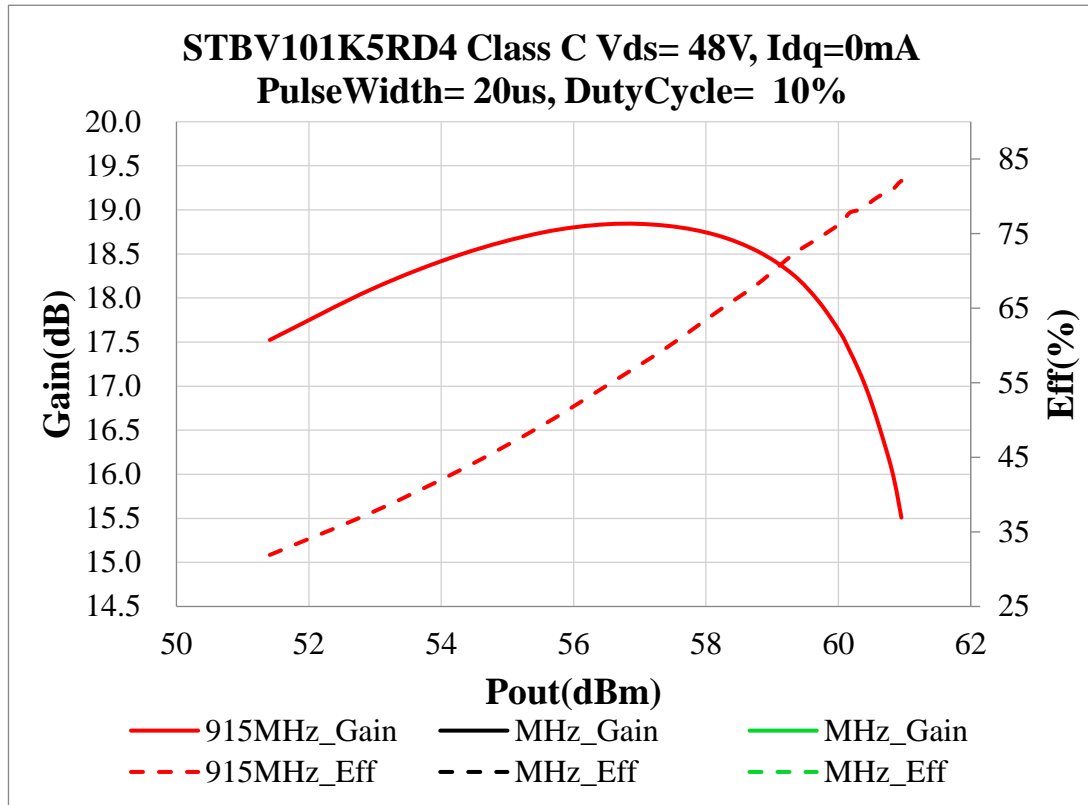
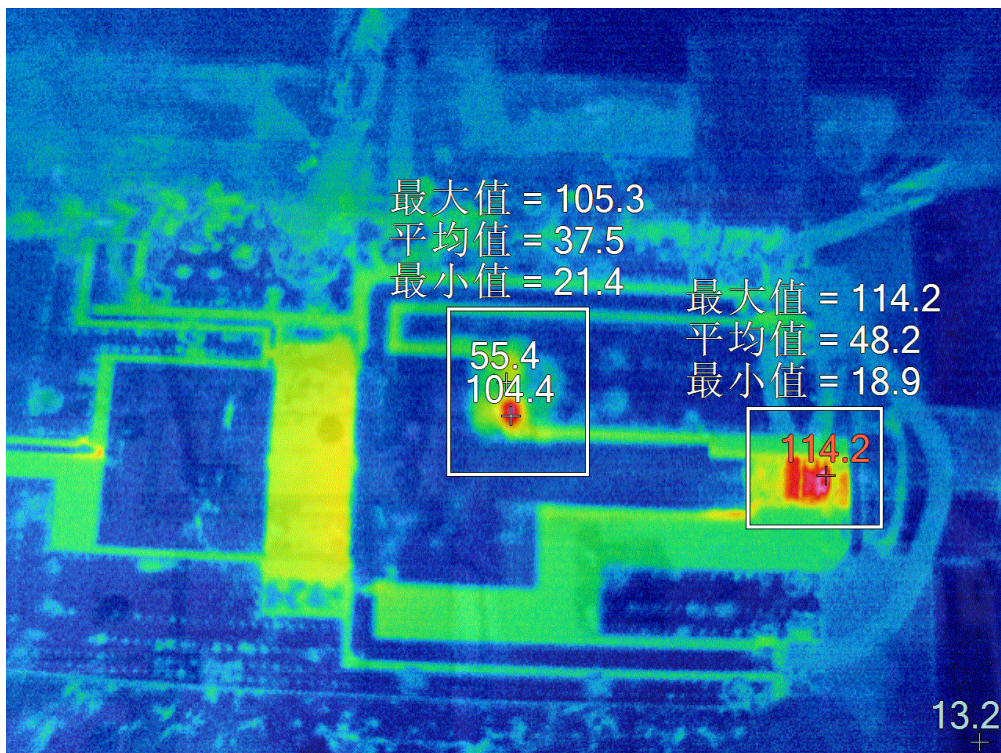


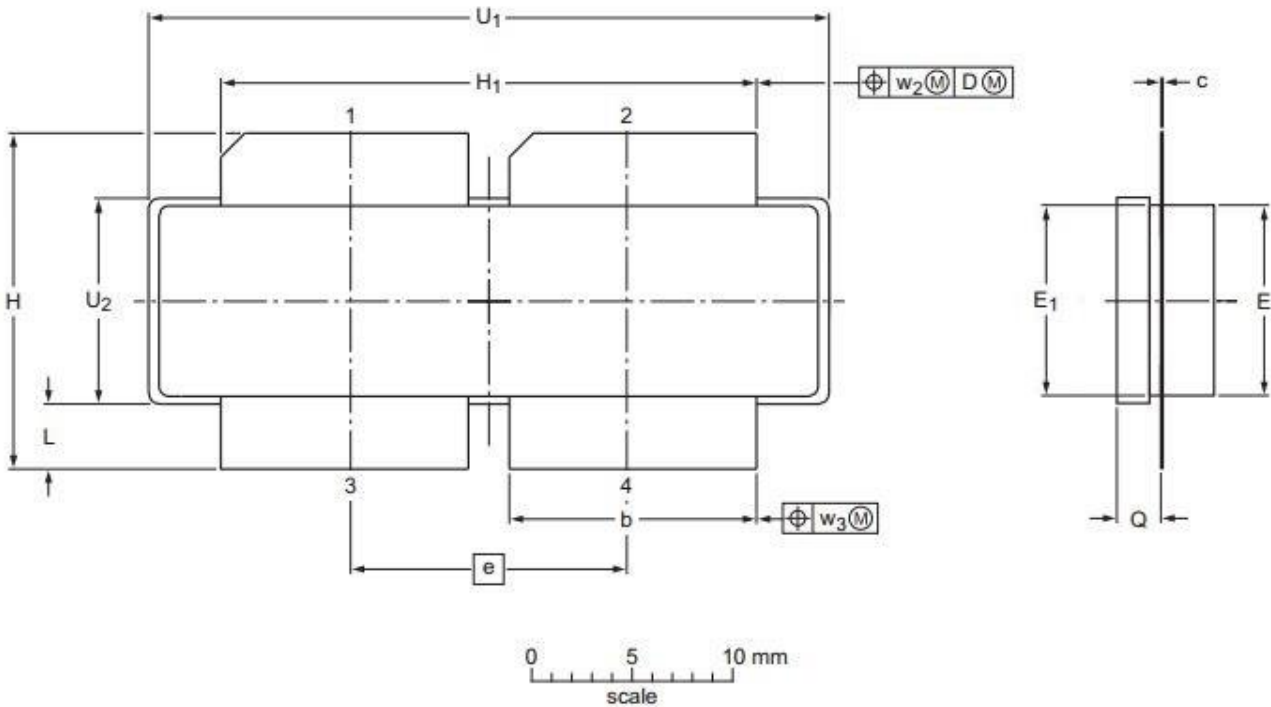
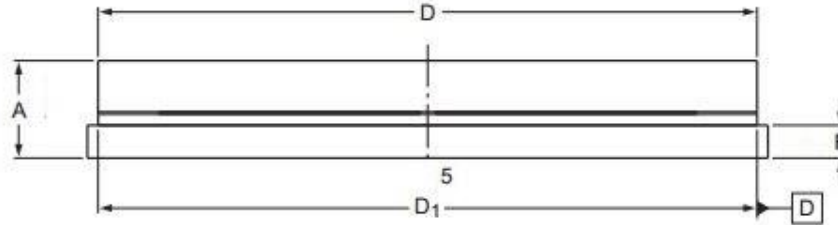
Figure 4: Thermal scan image on PCB when Pout=1000W CW





Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2024/1/29	Rev 1.0	Preliminary datasheet creation
2024/11/20	Rev 1.1	Add CW performance to state CW supportable

Application data based on: LSM-24-05

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